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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/822,302	04/09/2004	Ansheng Liu	42P14583D	2346	
7590 03/24/2005			EXAMINER		
Cory G. Claassen			DONG, DALEI		
BLAKELY, SC	KOLOFF, TAYLOR &	ZAFMAN LLP			
Seventh Floor			ART UNIT	PAPER NUMBER	
12400 Wilshire Boulevard			2879		
Los Angeles, CA 90025			DATE MAILED, 02/04/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

				M .F
Office Action Summary		Application No.	Applicant(s)	
		10/822,302	LIU ET AL.	
		Examiner	Art Unit	
		Dalei Dong	2879	
Period fo	The MAILING DATE of this communication ap	pears on the cover sheet	with the correspondence address	
A SH THE - Exte after - If the - If NC - Failu Any	IORTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. In SIX (6) MONTHS from the mailing date of this communication. The period for reply specified above is less than thirty (30) days, a repl period for reply is specified above, the maximum statutory period ure to reply within the set or extended period for reply will, by statut reply received by the Office later than three months after the mailing led patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may oly within the statutory minimum of t will apply and will expire SIX (6) Mine, cause the application to become	a reply be timely filed hirty (30) days will be considered timely. ONTHS from the mailing date of this communication ABANDONED (35 U.S.C. § 133).	cation.
Status				
1)⊠	Responsive to communication(s) filed on <u>07 F</u>	ebruary 2005.		
2a)⊠	This action is FINAL . 2b) Thi	s action is non-final.		
3)	Since this application is in condition for allows	·	•	ts is
	closed in accordance with the practice under	Ex parte Quayle, 1935 C	.D. 11, 453 O.G. 213.	
Disposit	ion of Claims			
5)□ 6)⊠ 7)□	Claim(s) 1-11 and 15-17 is/are pending in the 4a) Of the above claim(s) 15-17 is/are withdra Claim(s) is/are allowed. Claim(s) 1-11 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/	wn from consideration.		
Applicat	ion Papers			
10)⊠	The specification is objected to by the Examin The drawing(s) filed on <u>09 April 2004</u> is/are: a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Examin The specification is objected to be specification.	a)⊠ accepted or b)□ ob e drawing(s) be held in abey ction is required if the drawi	rance. See 37 CFR 1.85(a). ng(s) is objected to. See 37 CFR 1.1	
Priority	under 35 U.S.C. § 119			
a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau See the attached detailed Office action for a list	nts have been received. Its have been received in ority documents have been received in the later of the later (PCT Rule 17.2(a)).	Application No en received in this National Stage	e
2) Notice 3) Infor	nt(s) ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) rmation Disclosure Statement(s) (PTO-1449 or PTO/SB/08 er No(s)/Mail Date	Paper N	w Summary (PTO-413) o(s)/Mail Date If Informal Patent Application (PTO-152)	

U.S. Patent and Trademark Office PTOL-326 (Rev. 1-04)

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 15-17 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-11 are, drawn to a system, classified in class 385, subclass 37.
- II. Claims 15-17 are, drawn to a method of operating the system, classified in class 385, subclass 14.

Inventions of Group I and Group II are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case the system of invention of Group I can be operated using a different method as cited in U.S. Patent No. 6,317,538 to Shigehara. Invention of Group II is classified in a different class and subclass, therefore provides extra burden upon the Examiner and thus restriction is proper. The criteria for establishment of restriction is if it can be shown that the apparatus can be manufactured by an entirely different method as claimed by applicant. Because the method of making and the apparatus of an organic light-emitting panel are distinct invention as acquired a separate status in the art as shown by their different classification, restriction for examiner purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventor is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 15-17 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

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Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,343,167 to Scalora in view of U.S. Patent No. 5,801,378 to Hane.

Regarding to claim 1, Scalora discloses in Figure 7, a system comprising: an optical signal source (704); and an integrated circuit (708) operatively coupled (via fiber optic cable 706) to the optical signal source (704).

However, Scalora does not disclose the integrated circuit including a substrate and a plurality of regions formed in the substrate. Hane teaches in Figure 3, a substrate (38); and a plurality of regions (36 or transparent regions) formed in the substrate and having refractive indices (transparent) different from that of the substrate (non-transparent), the plurality of regions and intervening areas of the substrate (38) to form a grating, the grating having a plurality of grating period with substantially constant pitch (P), wherein each grating periods of the plurality of grating periods includes a region of the plurality of regions, the plurality of regions having regions of at least two different width (36-0 is 23P/30; 36-1 is 17P/30; 36-2 is 7P/30 and 36-3 is 13P/30) (see column 8, lines 5-51) for the purpose of achieve a stable sine wave displacement signal with low distortion where

the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the integrated circuit having plurality of regions of Hane for the system of Scalora in order to achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

Regarding to claim 2, Hane teaches in Figure 3, for each grating period (36-0) of the plurality of grating periods, a grating period (36-1) adjacent to that grating period (36-0) has a region having a width different from the width of that grating period's region (see column 8, lines 4-21).

Regarding to claim 3, Scalora discloses in Figures 4A and 6A, fiber grating with alternating layers of materials or sections having different indices of refraction periodically spaced on a substrate.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,343,167 to Scalora in view of U.S. Patent No. 5,801,378 to Hane and in further view of U.S. Patent No. 6,459,533 to Clapp.

Regarding to claim 4, Scalora discloses in Figure 7, a system comprising: an optical signal source (704); and an integrated circuit (708) operatively coupled (via fiber optic cable 706) to the optical signal source (704).

However, Scalora does not disclose the integrated circuit including a substrate and a plurality of regions formed in the substrate and the plurality of regions is formed from ploysilicon and the substrate is formed from crystalline silicone. Hane teaches in Figure 3, an integrated circuit (32) including: a substrate (38); and a plurality of regions (36 or transparent regions) formed in the substrate and having refractive indices (transparent) different from that of the substrate (non-transparent), the plurality of regions and intervening areas of the substrate (38) to form a grating, the grating having a plurality of grating period with substantially constant pitch (P), wherein each grating periods of the plurality of grating periods includes a region of the plurality of regions, the plurality of regions having regions of at least two different width (36-0 is 23P/30; 36-1 is 17P/30; 36-2 is 7P/30 and 36-3 is 13P/30) (see column 8, lines 5-51) for the purpose of achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

Clapp teaches the plurality of regions are formed from polysilicon and the substrate is formed from crystalline silicone (column 3, lines 16-60) for the purpose of achieving a fast response from the integrated circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the integrated circuit having plurality of regions of

Hane for the system of Scalora and construct the plurality of regions from ploysilicon and the substrate from crystalline silicone in accordance to Clapp in order to achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,343,167 to Scalora in view of U.S. Patent No. 5,801,378 to Hane and in further view of U.S. Patent No. 6,075,908 to Paniccia.

Regarding to claim 5, Scalora discloses in Figure 7, a system comprising: an optical signal source (704); and an integrated circuit (708) operatively coupled (via fiber optic cable 706) to the optical signal source (704).

However, Scalora does not disclose the integrated circuit including a substrate and a plurality of regions formed in the substrate and the plurality of regions is formed proximate to a buried insulator layer of a silicon-on-insulator (SOI) wafer. Hane teaches in Figure 3, an integrated circuit (32) including: a substrate (38); and a plurality of regions (36 or transparent regions) formed in the substrate and having refractive indices (transparent) different from that of the substrate (non-transparent), the plurality of regions and intervening areas of the substrate (38) to form a grating, the grating having a plurality of grating period with substantially constant pitch (P), wherein each grating periods of the plurality of grating periods includes a region of the plurality of regions, the plurality of

regions having regions of at least two different width (36-0 is 23P/30; 36-1 is 17P/30; 36-2 is 7P/30 and 36-3 is 13P/30) (see column 8, lines 5-51) for the purpose of achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

Paniccia teaches in Figure 3, the plurality of regions is formed proximate to a buried insulator layer of a silicon-on-insulator wafer (see column 7, lines 11-26) for the purpose of increase the modulation depth, and reduce the impact on other optical components in the apparatus.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the plurality of regions or transparent regions of Hane proximate to a buried insulator layer of a silicon-on-insulator wafer of Paniccia and utilize it in the system of Scalora in order to achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings and increase the modulation depth, and reduce the impact on other optical components in the apparatus.

6. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,343,167 to Scalora in view of U.S. Patent No. 5,801,378 to Hane and in further view of U.S. Patent No. 5,195,161 to Adar.

Regarding to claim 6, Scalora discloses in Figure 7, a system comprising: an optical signal source (704); and an integrated circuit (708) operatively coupled (via fiber optic cable 706) to the optical signal source (704).

However, Scalora does not disclose the integrated circuit including a substrate and a plurality of regions formed in the substrate and forming a cladding layer on the substrate and the plurality of regions. Hane teaches in Figure 3, an integrated circuit (32) including: a substrate (38), and a plurality of regions (36 or transparent regions) formed in the substrate and having refractive indices (transparent) different from that of the substrate (non-transparent), the plurality of regions and intervening areas of the substrate (38) to form a grating, the grating having a plurality of grating period with substantially constant pitch (P), wherein each grating periods of the plurality of grating periods includes a region of the plurality of regions, the plurality of regions having regions of at least two different width (36-0 is 23P/30; 36-1 is 17P/30; 36-2 is 7P/30 and 36-3 is 13P/30) (see column 8, lines 5-51) for the purpose of achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings.

Adar teaches in Figures 2 and 5, a cladding layer (14) on the substrate (11) and the plurality of regions (13) (see column 3, lines 34-65) for the purpose of protecting from impurities and prevents external force from damaging the plurality of regions.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have add a cladding layer of Adar to the substrate or non-

transparent region and the plurality of regions or transparent regions of Hane and utilize the waveguide for the system of Scalora in order to achieve a stable sine wave displacement signal with low distortion where the fundamental wave component of the output signal of the displacement signal is independent of the gap between the two diffraction gratings and provide protection from impurities and prevents external force from damaging the plurality of regions.

Regarding to claim 7, Adar teaches in Figures 2 and 5, a rib waveguide (13) is formed in the substrate (11), the rib waveguide containing the plurality of regions and the motivation to combine is the same as above.

Regarding to claim 8, Adar teaches the substrate and the plurality of regions form a Bragg grating and the motivation to combine is the same as above.

Regarding to claim 9, Hane in view of Adar disclose the claimed invention except for the specific claimed ranges of number of Bragg grating and extinction ratio. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have adjust the number of Bragg grating and the extinction ratio in accordance to the design specification, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Regarding to claim 10, Scalora discloses in Figure 8, the waveguide Bragg grating's Bragg wavelength is electronically tunable (see column 11, lines 21-39).

Regarding to claim 11, Scalora discloses in Figure 7, the waveguide Bragg grating's Bragg wavelength is thermally tunable.

Response to Arguments

7. Applicant's arguments filed February 7, 2005 have been fully considered but they are not persuasive.

In response to Applicant's argument that the Hane reference fails to teach or suggest an integrated circuit as claimed by the Applicant. The Applicant also argues that the definition of the integrated circuit is "a tiny complex electronic components and their connections that is produced in or on a small slice of material". The Examiner asserts that the Scalora reference clearly teaches in integrated circuit in Figure 8, wherein the plurality of different regions within the substrate each represents a separate electronic component and they are interconnected to produce a Fabry-Perot delay line device or an integrated circuit.

Also, the definition of an integrated circuit as claimed by the Applicant in the claim merely includes a substrate and a plurality of regions formed in the substrate, there are no mention whatsoever of any electronic components in the claim. Therefore, the Examiner given the broadest interpretation that the integrated circuit according to the

claim includes a substrate and a plurality of regions formed in the substrate as taught by the Hane reference. Thus, the Examiner asserts that the prior art of record teaches the claimed invention and maintains the rejection.

Further, in response to Applicant's argument that the Paniccia reference cannot be relied upon for the 103(a) rejection. The Examiner asserts that albeit Paniccia reference and the present application have a common assignee, however, Paniccia reference was issued on June 13, 2000, which is more than two years prior to the filing of the present application. Therefore, Paniccia reference is a 102(b) reference and does not subject to 103(c) requirements. Thus, the Examiner asserts that the Paniccia reference is valid in the 103(a) rejection and maintains the rejection.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

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advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (571)272-2370. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571)272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 16, 2005

Joseph Williams Primary Examiner Art Unit 2879

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